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EXAMINER	
PARENDO, KEVIN A	
ART UNIT	**PAPER NUMBER**
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,303	KNECHTEL, ROY	
	Examiner	Art Unit	
	Kevin Parendo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) *11-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/14/11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/13/11 has been entered.

Claim Objections

2. Claims 1 and 22 are objected to because “middle position” should be amended to “central area” in order to better match the specification’s language in paragraph 10 of the published application.

3. Claim 1 is objected to because “electrically conducting glass pastes” on lines 11-12 should be amended to “the electrically conducting glass paste” for proper antecedent basis.

4. Claims 1 and 22 are objected to because “joining” on lines 15 and 17, respectively, should be amended to “bonding” in order to better match the specification’s language in paragraph 33 of the published application.

5. Claims 1 and 22 are objected to because “wafer sides” on line 10 of claim 1 and lines 11 and 14 of claim 22 lack proper antecedent basis. The preceding limitation is “wafer surfaces”. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-9, 21, and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter (i.e. “new matter”) that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 has been amended to recite, and new **claim 22** recites, the limitation "providing an electrically non-conducting glass paste comprising glass particles and a binder and an electrically conducting glass paste comprising glass particles and a binder”.

According to MPEP 2163(II)(A), "with respect to newly added or amended claims, applicant should show support in the original disclosure for the new or amended claims.” This section also points to MPEP 714.02, 2163.06, and 2163.04. Applicant has not done this. The word “binder” does not occur anywhere in the originally filed specification, claims, or drawings. Rather, the applicant refers to a reference “FERRO”

and a reference "Lee" (see page 9 of remarks that were submitted on 4/13/11), arguing that "the fact that glass paste 'comprises glass particles and organic vehicle' (binder) is again just a definition of glass paste as is apparent from the citation 'Ferro'... The same definition is also given in the US 6,183,871 B1 abstract, where it is stated that sealing glass paste comprises at least one sealing glass frit powder and a binder which may comprise an emulsion of a polymeric material". This is not adequate to prevent a new matter rejection, because the glass particles and binder are not inherent, nor are included by definition.

While Lee's glass paste includes a binder and glass particles, it has not been shown that the applicant possessed these limitations at the time of original filing. In fact, the applicant uses the terms "glass frit bonding" (paragraphs 2 and 9), "glass paste" (paragraphs 16, 28, and 30), and "glass solders" (paragraphs 17, 21, 22, 24, 26). The different terms create confusion as to exactly the nature of the glass material that was originally envisioned by the applicant. Not all "glass bonding" applications include a binder, as taught by US 6,609,940 B1 ("Seibold"), see column 3, lines 21-23, wherein "binder-free glass solder/glass powder can also be used in the case of pressing". The applicant's specification (a) uses some type of glass, which is not clear, (b) does not discuss a binder anywhere, and (c) claims "joining… using a mechanical pressure". It is certainly possible that the applicant intended a use similar to Seibold, which does not include a binder and uses pressure; it is also possible that the applicant did intend a glass paste having a binder, but there is no support in the originally filed specification to support that possibility. Thus, the new limitations are new matter.

Claims 2-9 and 21 depend from claim 1 and inherit its deficiencies.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-9, 21, and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation “conditioning and pre-melting the electrically non-conducting glass paste and electrically conducting glass pastes” on lines 11-12. **Claim 22** recites these conditions in two different steps, requiring “conditioning and pre-melting the electrically non-conducting glass paste" on line 10 and “conditioning and pre-melting the electrically conducting glass paste" on line 13.

The metes and bounds of the claims can not be determined for the following reasons: neither these claims, nor any dependent claim therefrom, nor the specification, describes in clear detail what “conditioning" refers to. The specification discusses “conditioning” only in paragraphs 19, 29, and 31 of the published application, and does not elaborate other than describing that it is done “in the customary extent and the customary processes”. This term is so vague (it is defined by Merriam Webster Dictionary as "to put into a proper state for work or use") that one of ordinary skill in the art would not understand, exactly, the scope of the invention. There are multiple possibilities of what “conditioning" may refer to: (1) forming the glass paste into a

specific shape in a specific location; (2) mixing a glass frit with a solvent to further form the glass paste, as discussed in Ristic; and (3) mixing the glass paste after it has been formed or applied so that its constituent solvent and glass particles are well mixed. There are even other possibilities the examiner can imagine (“silver paint” pastes often involve pumping the paste in a vacuum to rid the paste of dissolved air particles, so that they do not form voids when the paste is applied; it is possible that Ristic's conductive frit that has silver adhesive would be similarly conditioned).

If the language of a claim, considered as a whole in light of the specification and given its broadest reasonable interpretation, is such that a person of ordinary skill in the relevant art would read it with more than one reasonable interpretation, then a rejection of the claims under 35 U.S.C. 112, second paragraph, is appropriate. See MPEP 2173.05(a), MPEP 2143.03(I), and MPEP 2173.06. Thus, because this term is not specific and is not defined or discussed in the specification, it is completely necessary for the examiner or a person of ordinary skill in the art to imagine what might be intended by "conditioning", and thus the scope of the claim is unclear.

Furthermore, the metes and bounds of the claimed limitation can not be determined for the following reasons: neither this claim, nor any dependent claim therefrom, nor the specification, describes in clear detail what "premelting” refers to. Because there is no standard definition for “premelting” or “premelt” (for instance, it is not defined by Merriam Webster Dictionary or the Academic Press Dictionary of Science and Technology), one must attempt to guess as to what is meant. Because “pre” means before, the examiner can guess two possibilities: (1) a melting that occurs before

some other event; (2) an event related to a melting process that occurs before melting. The specification only discusses the “premelting” in paragraphs 17, 18, 29, and 31, and none of these discusses what is meant by premelting or what occurs during this process.

If the language of a claim, considered as a whole in light of the specification and given its broadest reasonable interpretation, is such that a person of ordinary skill in the relevant art would read it with more than one reasonable interpretation, then a rejection of the claims under 35 U.S.C. 112, second paragraph, is appropriate. See MPEP 2173.05(a), MPEP 2143.03(I), and MPEP 2173.06. Thus, because this term is not specific and is not defined or discussed in the specification, it is completely necessary for the examiner or a person of ordinary skill in the art to imagine what might be intended by "premelting", and thus the scope of the claim is unclear.

Claims 2-9 and 21 depend from claim 1 and inherit this deficiency.

In light of the aforementioned rejections of the claim(s) under 35 U.S.C. 112, the subsequent rejections under 35 U.S.C. 102 and/or 103 are based on prior art that reads on the interpretation of the claim language of the instant application as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The examination guidelines for determining obviousness under 35 U.S.C. 103 are described in MPEP 2141-2145.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-8, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,094,969 ("Warren") in view of US 5,545,912 ("Ristic") and US 6,817,917 B1 ("Kado").

Re claim 1, Warren discloses a process, wherein at least two processed semiconductor wafers (both **10**'s, see Fig. 2) having electrically active structures thereon (IC's **20**, see column 2, line 47 and Fig. 2) are located in a middle position of a stack of wafers (the stack consists of both **10**'s and **28**'s, see Fig. 2), and wherein in an operation of a mechanical connecting, electrically insulating connections **24** (column 2, line 68 – column 3, line 3; column 3, lines 63-65; and Figs. 1-2) and electrically conductive connections **25** (column 3, lines 21-24 and 62-63 and Figs. 1-2) are produced between said at least two processed semiconductor wafers each one thereof having a wafer surface side to be connected, said process comprising:

- providing an electrically non-conducting glass paste **24** (column 2, line 68 – column 3, line 1; this is called a “glass frit”, which is synonymous with “glass paste” because glass frit are the glass particles which, when screen printed, are dispersed in a solvent, thus being considered equivalent to a "paste"; for support for this statement, see Ristic, column 2, lines 23-32) comprising glass particles and an electrically conducting glass paste **25** (column 3, lines 21-24; also called a “glass frit”) comprising glass particles;
- applying patterned layers (each of **24** and **25** is patterned to cover specific elements, see column 3, lines 1-3, 9, 21, and 39) of the electrically non-conducting paste and the electrically conducting glass paste on said wafer surface sides (see Fig. 2);
- thereafter conditioning and pre-melting (column 3, lines 42-49) the electrically non-conducting glass paste and electrically conducting glass pastes;
- thereafter providing geometrical alignment of the at least two processed semiconductor wafers to be connected (they are aligned so that the electrical contacts between wafers through the electrically conductive glass exist, see column 3, lines 64-65);
- thereafter joining the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste and at a second processing temperature of the electrically conducting glass paste (they are joined at either 380 degrees or 480 degrees, depending on

the specific glass frit used, see column 3, lines 60-65; note, the claimed first and second temperatures need not be different, as the applicant uses them as the same temperature in claim 4) using a mechanical pressure (they are "stacked upon each other to form a sandwiched construction", see column 3, lines 50-52).

Warren does not disclose the "binder".

Ristic discloses a "binder" (column 2, line 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Ristic to the invention of Warren.

The motivation to do so is that the combination produces the predictable results of using an organic binder or solvent which may evaporate when heated, to disperse the glass particles so that they may be applied by screen printing (column 2, lines 23-31).

Warren does not disclose "processed semiconductor wafers" in one strict definition of wafer (being a semiconductor slab). Warren's wafers are "multi-layered substrates" (column 1, line 15-16) being a ceramic circuit board (column 1, lines 44-46 and 58-60). However, it is well known to store ICs and other devices between processed semiconductor wafers.

For example, Ristic discloses (see Figs. 1-2) bonding semiconductor substrate **12** (column 2, lines 12-13) to semiconductor cap **16** (column 2, lines 15-16 and column 3, lines 21-24) using insulating or conducting glass frit **14** (column 2, lines 23-32 and

column 3, lines 41-48) so that devices **26** (column 2, line 15) are enclosed in cavities **18** (column 2, line 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Ristic to the invention of Warren.

The motivation to do so is that the combination produces the predictable results of bonding not only ICs but other devices (such as 26), in a situation where conductive substrates (column 2, lines 12-13 and 15-16) may be joined so that electrical connections between them may be made (column 3, lines 18-14 and 44-48). This is useful for specific device types, such as accelerometers (column 3, line 64) or transistors, resistors, capacitors, inductors, transducers, or surface acoustic wave devices (column 5, lines 30-32) that may require hermetic sealing (column 2, line 18) in a cavity to provide EMI shielding (column 5, lines 44-46).

Thus, herein, when “semiconductor wafers” is discussed in terms of Warren, it is to be understood that the semiconducting materials of Ristic are being substituted for the ceramic circuit boards. This avoids the need for repetition of the above paragraph.

Warren does not explicitly disclose “conditioning and premelting of the electrically non-conducting glass pastes and the electrically conducting glass paste” using these terms “conditioning” and “pre-melting”. However, the examiner notes the rejection of the claims under the second paragraph of 112, above, for the ambiguity of these limitations. The examiner notes that the conditioning is disclosed by the Applicant to be "customary" (paragraph 19 of the published application). It is therefore an obvious

condition for one of ordinary skill in the art to apply. It is reasonable to interpret the preparation of a first substrate 10 (column 3, lines 42-49) as "conditioning" by placing it in an oven; it is reasonable to interpret the baking (lines 45-47) as a "pre-melting" because it is pre-completion of the multistacked substrate structure (column 3, line 66).

Also, for example, the mixing of the glass frit and solvent together to form the paste (Ristic, column 2, lines 23-32) can be considered "conditioning". Warren's mixing in the silver adhesive (column 3, lines 17-20) only in the conducting paste may be interpreted as "conditioning" that is different than the "conditioning" of the non-conducting paste. Thus, the "conditioning" limitation would be obvious to one of ordinary skill in the art.

Regarding the "premelting", Kado discloses "pre-baking" glass frit at 350 degrees (column 7, lines 45-49 and column 16, lines 16-21). This is interpreted as “premelting” because it is a heating process conducted before the melting.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kado to the invention of Warren and Ristic.

The motivation to do so is that the combination produces the predictable results of heating the glass paste so that resin and other materials are removed (column 7, lines 45-49 and column 16, lines 16-21).

Re claim 2, Warren further discloses that the electrically non-conducting glass paste and the electrically conducting glass paste are applied by a screen printing process (column 3, line 39).

Re claim 3, Warren and Ristic disclose the limitations of claim 1, as discussed above. Neither Warren or Ristic further discloses that the electrically non-conducting glass paste and the electrically conducting glass paste have different conditioning conditions and premelting conditions and, therefore, the conditioning and the premelting are implemented successively, each in a separate conditioning and premelting process.

The examiner notes the rejection of the claims under the second paragraph of 112, above, for the ambiguity of the "conditioning" limitation. The examiner notes that the conditioning is disclosed by the Applicant to be "customary" (paragraph 19 of the published application). It is therefore an obvious process for one of ordinary skill in the art to perform. For example, the mixing of the glass frit and solvent together to form the paste (Ristic, column 2, lines 23-32) can be considered "conditioning". And this, together with Warren's mixing in the silver adhesive (column 3, lines 17-20) only in the conducting paste may be interpreted as "conditioning" that is different than the "conditioning" of the non-conducting paste.

Regarding the "premelting", the examiner notes the ambiguity regarding this term, as discussed above with the 112 rejection. Kado discloses "pre-baking" glass frit at 350 degrees (column 7, lines 45-49 and column 16, lines 16-21). This is interpreted as “premelting” because it is a heating process conducted before the melting. It also appears to be a well known process that is part of a general “conditioning” that occurs while using glass pastes in the prior art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kado to the invention of Warren and Ristic.

The motivation to do so is that the combination produces the predictable results of heating the glass paste so that resin and other materials are removed (column 7, lines 45-49 and column 16, lines 16-21).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a process such that the electrically non-conducting glass paste and the electrically conducting glass paste have different conditioning conditions and premelting conditions (since Warren adds silver adhesive to the areas that are conductive, the conductive portion would have different physical properties and thus different conditioning and premelting properties) and, therefore, the conditioning process and the premelting process are implemented successively, each in a separate conditioning and premelting process (if they both have different conditions, it is necessary to perform them successively, because it would not be possible to perform them simultaneously).

Re claims 4 and 5, Warren does not disclose explicitly that

- that the first processing temperature of the electrically non-conducting glass paste and the second processing temperature of the electrically conducting glass paste are “the same processing temperature” (**claim 4**); or that

- the first processing temperature of the electrically non-conducting glass paste and the second processing temperature of the electrically conducting glass paste are "different processing temperatures" and wherein the first processing temperature and the second processing temperature are successively passed in the process of joining the at least two processed semiconductor wafers (**claim 5**).

Rather, Warren discloses that both **24** and **25** are heated to either 380 or 480 degrees, depending on which type of glass frit is used (see column 3, lines 44-47). Thus, both **24** and **25** are made of the same glass frit. They then have the same "processing temperature" if it is interpreted as the temperature at which both frits are heated to and that is sufficient to melt both frits. This thus renders claim 4 unpatentable.

The non-conductive frit is made to be conductive by adding silver/glass conducting adhesive (see column 3, lines 17-20) in specific areas where conductive frit is desired. If "processing temperature" is interpreted as a "melting temperature", then one of ordinary skill in the art at the time of invention would understand that since the frits began as the same, with the same melting temperature, that adding another adhesive composition to the frit to make it conductive would alter its physical properties including its melting temperature. Thus, they would have "different processing temperatures". Warren then heats to a higher processing temperature (e.g. 480) that is sufficient to melt both frits. Warren thus would have to successively pass both melting temperatures by during the connecting/joining.

Re claim 6, Warren further discloses that at least one of the at least two processed semiconductor wafers has an electrical connection in an area that does not contain electronic structures (see column 3, lines 21-24, wherein the substrates are connected electrically, but not the ICs).

Re claim 7, Warren further discloses that the at least two processed semiconductor wafers are electrically connected at specific electric circuit points in areas containing electronic structures (see column 1, line 64 - column 2, line 5, wherein "the ICs may be electrically connected between the stacked boards").

Re claim 8, Warren further discloses that the joining of the at least two processed semiconductor wafers further comprises the first processing temperature and the second processing temperature being about 450°C (they are joined at either 380 degrees or 480 degrees, depending on the specific glass frit used, see column 3, lines 43-49 and 60-65).

Re claim 21, Warren further discloses that the applying of the patterned layers comprises applying a first patterned layer of the electrically non-conducting glass paste to the wafer surface side of a first one of the at least two processed semiconductor wafers (see column 1, lines 63-65, wherein the non-conducting glass frit is formed to cover “each individual" wafer; see column 2, line 67 – column 3, line 3, wherein the ICs

20 may be covered, but only one of which is shown; thus, both sides of each **10** are covered with **24**) and applying a second patterned layer of the electrically conducting glass paste on the wafer surface side of a second one of the at least two processed semiconductor wafers (when **25** is made to be conductive in some selected area, is necessarily is either on the top or bottom of a wafer **10**; thus, there will be **24** on one side of one wafer **10**, and there will be **25** on the opposite side of an adjacent wafer **10**).

Re claim 22, Warren discloses a process, wherein at least two processed semiconductor wafers (both **10**'s, see Fig. 2) having electrically active structures thereon (IC's **20**, see column 2, line 47 and Fig. 2) are located in a middle position of a stack of wafers (the stack consists of both **10**'s and **28**'s, see Fig. 2), and wherein in an operation of a mechanical connecting, electrically insulating connections **24** (column 2, line 68 – column 3, line 3; column 3, lines 63-65; and Figs. 1-2) and electrically conductive connections **25** (column 3, lines 21-24 and 62-63 and Figs. 1-2) are produced between said at least two processed semiconductor wafers each one thereof having a wafer surface side to be connected, said process comprising:

- providing an electrically non-conducting glass paste **24** (column 2, line 68 – column 3, line 1; this is called a "glass frit", which is synonymous with "glass paste" because glass frit are the glass particles which, when screen printed, are dispersed in a solvent, thus being considered equivalent to a "paste"; for support for this statement, see Ristic, column 2, lines 23-32) comprising glass

particles and an electrically conducting glass paste **25** (column 3, lines 21-24; also called a "glass frit") comprising glass particles;

- applying a patterned layer (each of **24** and **25** is patterned to cover specific elements, see column 3, lines 1-3, 9, 21, and 39) of the electrically non-conducting paste on said wafer surface sides (see Fig. 2);
- thereafter (after applying **24**, as discussed above) conditioning and pre-melting (column 3, lines 42-49) the electrically non-conducting glass paste and electrically conducting glass pastes;
- applying a patterned layer (each of **24** and **25** is patterned to cover specific elements, see column 3, lines 1-3, 9, 21, and 39; these may be simultaneous with each other, as the claim does not require applying **24** and **25** at separate times) of electrically conducting glass paste on said wafer surface sides (see Fig. 2);
- thereafter (after applying **25**, as discussed above) conditioning and pre-melting (column 3, lines 42-49) the electrically conducting glass paste on said wafer sides;
- thereafter providing geometrical alignment of the at least two processed semiconductor wafers to be connected (they are aligned so that the electrical contacts between wafers through the electrically conductive glass exist, see column 3, lines 64-65);
- thereafter joining the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste

and at a second processing temperature of the electrically conducting glass paste (they are joined at either 380 degrees or 480 degrees, depending on the specific glass frit used, see column 3, lines 60-65; note, the claimed first and second temperatures need not be different, as the applicant uses them as the same temperature in claim 4) using a mechanical pressure (they are "stacked upon each other to form a sandwiched construction", see column 3, lines 50-52).

Warren does not disclose the "binder".

Ristic discloses a "binder" (column 2, line 27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Ristic to the invention of Warren.

The motivation to do so is that the combination produces the predictable results of using an organic binder or solvent which may evaporate when heated, to disperse the glass particles so that they may be applied by screen printing (column 2, lines 23-31).

Warren does not disclose "processed semiconductor wafers" in one strict definition of wafer (being a semiconductor slab). Warren's wafers are "multi-layered substrates" (column 1, line 15-16) being a ceramic circuit board (column 1, lines 44-46 and 58-60). However, it is well known to store ICs and other devices between processed semiconductor wafers.

For example, Ristic discloses (see Figs. 1-2) bonding semiconductor substrate **12** (column 2, lines 12-13) to semiconductor cap **16** (column 2, lines 15-16 and column 3, lines 21-24) using insulating or conducting glass frit **14** (column 2, lines 23-32 and column 3, lines 41-48) so that devices **26** (column 2, line 15) are enclosed in cavities **18** (column 2, line 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Ristic to the invention of Warren.

The motivation to do so is that the combination produces the predictable results of bonding not only ICs but other devices (such as 26), in a situation where conductive substrates (column 2, lines 12-13 and 15-16) may be joined so that electrical connections between them may be made (column 3, lines 18-14 and 44-48). This is useful for specific device types, such as accelerometers (column 3, line 64) or transistors, resistors, capacitors, inductors, transducers, or surface acoustic wave devices (column 5, lines 30-32) that may require hermetic sealing (column 2, line 18) in a cavity to provide EMI shielding (column 5, lines 44-46).

Thus, herein, when “semiconductor wafers” is discussed in terms of Warren, it is to be understood that the semiconducting materials of Ristic are being substituted for the ceramic circuit boards. This avoids the need for repetition of the above paragraph.

Warren does not explicitly disclose “conditioning and premelting of the electrically non-conducting glass pastes and the electrically conducting glass paste” using these terms “conditioning” and “pre-melting”. However, the examiner notes the rejection of

the claims under the second paragraph of 112, above, for the ambiguity of these limitations. The examiner notes that the conditioning is disclosed by the Applicant to be "customary" (paragraph 19 of the published application). It is therefore an obvious condition for one of ordinary skill in the art to apply. It is reasonable to interpret the preparation of a first substrate 10 (column 3, lines 42-49) as "conditioning" by placing it in an oven; it is reasonable to interpret the baking (lines 45-47) as a "pre-melting" because it is pre-completion of the multistacked substrate structure (column 3, line 66).

Also, for example, the mixing of the glass frit and solvent together to form the paste (Ristic, column 2, lines 23-32) can be considered "conditioning". Warren's mixing in the silver adhesive (column 3, lines 17-20) only in the conducting paste may be interpreted as "conditioning" that is different than the "conditioning" of the non-conducting paste. Thus, the "conditioning" limitation would be obvious to one of ordinary skill in the art.

Regarding the "premelting", Kado discloses "pre-baking" glass frit at 350 degrees (column 7, lines 45-49 and column 16, lines 16-21). This is interpreted as “premelting” because it is a heating process conducted before the melting.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kado to the invention of Warren and Ristic.

The motivation to do so is that the combination produces the predictable results of heating the glass paste so that resin and other materials are removed (column 7, lines 45-49 and column 16, lines 16-21).

9. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Warren, Ristic, and Kado, as applied to claim 1, above, and further in view of US 2003/0170936 A1 ("Christensen").

Re claim 9, Warren, Ristic, and Kado disclose the limitations of claim 1, as discussed above, but fail to further disclose that one of the at least two processed semiconductor wafers is a SOI wafer comprising an active semiconductor layer and a buried oxide layer on a substrate and wherein an electrical connection to the substrate of the SOI wafer is implemented through previously produced openings in the buried oxide layer and in the active semiconductor layer.

Christensen discloses that one of the at least two processed semiconductor wafers is a SOI wafer (paragraph 2) comprising an active semiconductor layer and a buried oxide layer **106** or **108** (paragraph 20) on a substrate **104** (paragraph 20) and wherein an electrical connection to the substrate of the SOI wafer is implemented through previously produced openings **300** (Fig. 3 and paragraph 24) in the buried oxide layer **106 or 108** (Fig. 3) and in the active semiconductor layer **102** (Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Christensen to the invention of Warren, Ristic, and Kado.

The motivation to do so is that the combination produces the predictable results of connecting a SOI wafer with improved speed of signals (paragraph 2) to an external wafer.

Response to Arguments

10. Applicant's arguments with respect to the pending claims have been considered.

Regarding the 112 rejections:

The applicants argue that the inclusion of a “binder” in the claim is supported by a “definition" of a glass paste (see page 10 of remarks). This is not persuasive. First, Neither the FERRO reference nor the Lee reference defines all “glass pastes” as having a binder. Second, the applicant has used multiple terms for glass bonding, and the specification does not have support for a binder, so that it is not clear that the applicant intended at the time of filing to include a binder. It was shown above that not all glass bonding applications involve a binder (see the discussion above about the Seibold reference). Thus, a binder is not included by definition or inherency, and this is new matter. Arguments pertaining to the binder are thus unpersuasive.

Applicant’s arguments that stem from a binder are that "FERRO” discusses steps (1)-(5) (see page 10 of remarks), which talk about possible meanings of “conditioning” and “pre-melting”. This FERRO reference was published many years after the applicant's filing date, and is merely one reference that has one opinion that a specific glass paste (i.e. FERRO corporation’s 11-036, 11-155, and 11-201 “non-crystallizing thick film glass pastes designed for sealing") uses these five steps. However, it is merely one example. The Seibold reference shows other non-binder glass bonding applications, and thus since it is not clear that the applicant ever intended for a binder in the invention, it does not follow that FERRO is evidence for unambiguous clarity of the terms “conditioning" and "pre-melting”. At best, FERRO discusses only one example of

possible meanings of “conditioning” and “pre-melting”. FERRO thus, at best, only adds possible meanings to the possible meanings imagined by the examiner in the 112 rejection above. It does not supersede the examiner's possible meanings. It only thus adds to a list of possible meanings, and as discussed above, if more than one reasonable interpretation for a meaning is possible, the scope of the claim is unclear.

Applicants citation of Lee to support conditioning and pre-melting may allow for some possible examples of conditioning and pre-melting, but Lee does not limit all possible examples of conditioning and of pre-melting to those discussed in Lee; rather, these merely discuss one specific glass paste (Lee’s “sealing glass paste which overcomes the problems of the prior art", column 1, lines 65-66, to seal cathode ray tubes) add to the possible examples discussed by the examiner (see the 112 rejection above). Because more than one reasonable example is possible, the scope of these limitations is unclear.

Applicants make statements that the examiner does not agree with. Applicants state "the examiner admits that glass frit and glass paste are synonymous and define a material which consists out of glass particles and a binder" (page 10, middle of page). The examiner does not agree with this remark, and again repeats that the applicant has used at least three different terms for glass bonding, and there is support in the prior art for examples that do not need binders.

Applicants further argue that the “glass” terms used by the applicant are consistent with each other, as supported by the “SCHOTT” reference. This is not persuasive, because while the terms may be related or synonymous according to one

reference, it does not mean that it is so universally. The examiner has provided a reference in which a binder is not necessary. Thus, the conditioning and pre-melting do not necessarily refer to a binder, as now argued by the applicant but which lacks any support in the originally filed specification.

Regarding the 103 rejections:

The applicant argues that Warren, Ristic, and Kado do not disclose the limitations of claim 1 (see remarks, page 12). Applicants make a statement that both claims 1 and 22 claim the sequence of steps listed near the bottom of page 12, which is inaccurate. Claim 22 does not require "applying patterned layers of electrically non-conducting glass paste and electrically conducting glass paste on said wafer sides; thereafter conditioning and premelting the electrically non-conducting glass paste and electrically conducting glass paste" because claim 22 requires a different sequence (see lines 7-14).

The applicant makes statements that “Warren teaches forming a substrate” (page 12, last paragraph), and “the cover 16 of Ristic cannot be understood as a processed wafer” (page 13, second paragraph). The applicant has not defined what a “wafer" is, or what a “processed wafer” is. A wafer has a general definition as a thin supportive slab, which is equated with a substrate. A wafer has a semiconductor definition as a thin slice of a single crystal semiconductor. In the art, a wafer can not only be the thin slice, but can include deposited layers thereupon. "Processing" is a general term and can include cleaning, deposition, ion implanting, etching, etc. Warren

discloses the substrates **10** having electrically active structures thereon (Fig. 2) and Ristic discloses semiconducting substrates having electrically active structures thereon. It is obvious to use a semiconductor substrate of Ristic in place of the substrate of Warren, because Ristic allows for connection of not only ICs, but other types of devices. The applicant has not disclosed that the semiconducting wafer is unobvious or critical and could not instead be a generic substrate.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Parendo, whose can be contacted by phone at (571) 270-5030 or directly by fax at (571) 270-6030. The examiner can normally be reached on Mon.-Thurs. and alternate Fridays from 7 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin A. Parendo/
Examiner, Art Unit 2823
6/7/2011